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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/699,012	10/31/2003	Desmond Ambrose	015114-066100US	1423

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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/699,012	AMBROSE, DESMOND	
	Examiner	Art Unit	
	Aurangzeb Hassan	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/08/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. According to claim 22, the examiner acknowledges the dependencies as cited and urges the applicant to appropriately check proper dependencies for the aforementioned claim. The examiner notes claim 22 would be better dependant upon 21 rather than the claim 20 cited.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 15 and 16 recite the limitation "wherein the integrated circuit" in line 1 of both claims 15 and 16. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 thru 9 and 12 thru 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hershey et al. (US Publication Number 2001/0002199 hereinafter "Hershey").

6. Referring to claims 1 and 12, Hershey teaches an integrated circuit and a method comprising,

partially reconfigurable programmable circuit elements (FPGA page 3, paragraph [0027] line 16); and

a finite state machine (FSM page 4, paragraph [0048], line 14),

wherein the finite state machine configures the partially reconfigurable programmable circuit elements to detect boundaries between words in an input data stream (FSM Pattern Detector page 4, paragraph [0048]),

the finite machine state machine determines when the partially reconfigurable programmable circuit elements correctly indicates boundaries between frames in the input data stream (page 4, paragraphs [0048-0049]),

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align the words in the input data stream based on the detected word boundaries and to determine when the word boundaries have changed (control and management memory circuitry, element 130c of figure 2, paragraph [0048]).

7. Referring to claims 2 and 13, Hershey teaches an integrated circuit and a method comprising,

data and overhead processing circuitry (page 2, paragraph [0024], lines 9 – 14, synchronization, multiplexing, and control modules).

8. Referring to claims 3 and 14, Hershey teaches an integrated circuit and a method comprising,

input/output circuitry that receives the input data stream (figure 1, page 2, paragraphs [0022 – 0023]).

9. Referring to claims 4 and 15, Hershey teaches an integrated circuit and a method wherein, the integrated circuit includes portions of hardwired, application-specific circuitry.

10. Referring to claims 5 and 16, Hershey teaches an integrated circuit and a method wherein the integrated circuit is a field programmable gate array (figure 2, element 130a, FPGA, page 3, paragraph [0027], line 18).

11. Referring to claims 6 and 17, Hershey teaches an integrated circuit and a method wherein,

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate framing patterns in SONET input data (element 130a of figure 2 and FSM Pattern Detector page 4, paragraph [0048]).

The examiner notes use of the FPGA represents the reconfigurable programmable circuit upon which Hershey's FSM Pattern Detector is comprised. It is understood that which is claimed by Hershey in a high bandwidth multiplexing protocol, SONET, in one embodiment resides on FPGA hardware.

12. Referring to claims 7 and 18, Hershey teaches an integrated circuit and a method wherein,

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align frames in the SONET input data stream based on the detected boundaries (FPGA element 130a, figure 2, control and management memory circuitry, element 130c of figure 2, paragraph [0048]).

The examiner cites above interpretation of Hershey's invention explained for claims 6 and 17 and applies it to claims 7 and 18. Accordingly FPGA and control and management memory circuitry in Hershey's invention holds for claims 7 and 18.

13. Referring to claims 8 and 19, Hershey teaches an integrated circuit and a method wherein,

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate framing patterns in SDH frames in the input data stream (FPGA element 130a, figure 2 and FSM Pattern Detector page 4, paragraph [0048]).

Hershey's invention corresponds to both SONET and SDH communication protocols (Figure 1 element 19 SONET and/or SDH, paragraph [0023]). Accordingly the above explanation in reference to claims 6 and 17 for FPGA and FSM Pattern Detector in Hershey's invention holds for claims 8 and 19.

14. Referring to claims 9 and 20, Hershey teaches an integrated circuit and a method wherein,

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align frames in the SDH input data based on the detected boundaries (FPGA element 130a, figure 2, and control and management memory circuitry, element 130c of figure 2, paragraph [0048]).

Hershey's invention corresponds to both SONET and SDH communication protocols (Figure 1 element 19 SONET and/or SDH, paragraph [0023]). Accordingly the above explanation in reference to claims 7 and 18 for FPGA and control and management memory circuitry in Hershey's invention holds for claims 9 and 20.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 10, 11, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hershey in further view of Denton et al. (US Patent Number 6,567,413 hereinafter "Denton").

16. Referring to claims 10 and 21, Hershey teaches an integrated circuit and a method wherein,

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to locate training patterns (element 130a of figure 2 and FSM Pattern Detector page 4, paragraph [0048]).

However Hershey fails to teach the FSM Pattern Detector in OIF SPI4 phase 2 input data.

Denton teaches OIF SPI4 phase 2 input data stating the novelty of selecting SONET, SDH with OIF SPI4 phase 2 (column 6 lines 13 through 47). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Hershey with the above teachings of Denton. One of ordinary skill in the art would have been motivated to makes such modification in the FSM reconfiguration of the FPGA OIF SPI4 phase 2 training patterns based upon the understanding that SONET/SDH and OIF SPI4 phase 2 are employed hand in hand as suggested by Denton.

17. Referring to claims 11 and 22, Hershey in further view of Denton teaches an integrated circuit and a method wherein,

the finite state machine reconfigures the partially reconfigurable programmable circuit elements to align channels input data based on the detected training patterns (FPGA element 130a, figure 2, control and management memory circuitry, element 130c of figure 2, paragraph [0048]).

However Hershey fails to teach control and management memory circuitry in OIF SPI4 phase 2 input data.

Denton teaches OIF SPI4 phase 2 input data stating the novelty of selecting SONET, SDH with OIF SPI4 phase 2 (column 6 lines 13 through 47). It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Hershey with the above teachings of Denton. One of ordinary skill in the art would have been motivated to makes such modification in the FSM reconfiguration of the FPGA OIF SPI4 phase 2 alignments of channels based upon the understanding that SONET/SDH and OIF SPI4 phase 2 are employed hand in hand as suggested by Denton.

Conclusion

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aurangzeb Hassan whose telephone number is (571) 272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AH
11/29/2005

KIM HUYNH
PRIMARY EXAMINER
12/5/05